CLAIMS

1. A shift register circuit comprising a plurality of stages, each stage comprising an input section (60) and an output section (62), each stage being for providing a signal to an output load (64),

wherein the input section of each stage comprises an input section drive transistor (T_{drive}) for coupling a first clocked power line voltage (Pn) to the output of the input section (60), an input section compensation capacitor (C_1) for compensating for the effects of a parasitic capacitance of the input section drive transistor (T_{drive}) and a first input section bootstrap capacitor (C_2) connected between the gate of the drive transistor and the output of the input section,

wherein the input section (60) of each stage uses the output (R_{n-1}) of the input section (60) of at least one preceding stage as a timing control input for controlling a bootstrap function,

and wherein the output section (62) of each stage comprises a circuit which receives the outputs of multiple input sections (60) as timing signals for generating output signals for the output loads (64).

2. A circuit as claimed in claim 1, wherein the input section (60) of each stage further comprises:

a first input section input (R_{n-1}) connected to the output of the input section of a preceding stage; and

an input section input transistor (T_{in1}) for charging the first bootstrap capacitor (C_2) and controlled by the first input (R_{n-1}).

3. A circuit as claimed in claim 1 or 2, wherein the output of each output section (62) is used only for driving a respective output load

4. A circuit as claimed in any preceding claim, wherein the output section (62) comprises:

a first output section input (R_{n-1}) connected to the output of the input section of the preceding stage;

an output section drive transistor (T_{drive}) for coupling a first clocked power line voltage (Pn) to the output of the output section;

an output compensation capacitor (C_1) for compensating for the effects of a parasitic capacitance of the output section drive transistor (T_{drive});

a first output section bootstrap capacitor (C_2) connected between the gate of the drive transistor and the output of the stage; and

an output section input transistor (T_{in1}) for charging the first bootstrap capacitor and controlled by the first output section input.

5. A circuit as claimed in any preceding claim, wherein the input section (60) of each stage further comprises a portion (10) coupled to the output (R_{n-2}) of the input section stage two or more stages before the stage, and wherein the portion (10) comprises a second input section bootstrap capacitor (C_3) connected between the gate of the input section input transistor (T_{In1}) and the first input section input (R_{n-1}).

6. A circuit as claimed in any preceding claim, wherein the output section of each stage further comprises a portion (10) coupled to the output of (R_{n-2}) the input section stage two or more stages before the stage, and wherein the portion (10) comprises a second output section bootstrap capacitor (C_3) connected between the gate of the output section input transistor (T_{in1}) and the first output section input.

7. A circuit as claimed in any preceding claim, wherein the input section (60) of each stage further comprises a second input section input (R_{n+1}) connected to the output of the input section of the next stage.

8. A circuit as claimed in claim 7, wherein the second input section input (R_{n+1}) is connected to the gate of a reset transistor ($T_{r(n+1)}$) which is

connected between the gate of the input section drive transistor and a low power line.

9. A circuit as claimed in any preceding claim, wherein the input section compensation capacitor (C_1) of each stage is connected between the gate of the input section drive transistor and a second clocked power line voltage (invPn) which is clocked complementarily with the first power line voltage (Pn).

10. A circuit as claimed in claim 5, wherein the portion (10) comprises circuit elements for storing a transistor threshold voltage on the second input section bootstrap capacitor (C_3).

11. A circuit as claimed in claim 5, wherein the portion (10) further comprises:

a second input section input transistor (T_{in2}) which supplies the output of the stage two or more stages before the stage to the gate of the first input section input transistor (T_{in1}); and

a decay transistor (T_{decay}) connected in parallel with the second input section bootstrap capacitor (C_3) for decaying the voltage on the second input section bootstrap capacitor until the threshold voltage of the input section decay transistor is reached.

12. A circuit as claimed in claim 11, wherein the input section decay transistor has substantially the same dimensions as the first input section input transistor.

13. A circuit as claimed in claim 5, wherein the portion (10) further comprises a second input section input transistor (T_{in2}) which supplies the output of the stage two or more stages before the stage to the gate of the first input section input transistor (T_{in1}).

14. A circuit as claimed in claim 13, wherein the first input section input transistor (T_{in1}) is connected between an input line (L_{n-1}) and the gate of the input section drive transistor, and wherein the input line is high when output of the stage before is high, and is high at least immediately after the output of the input section of the stage before has a transition from high to low.

15. A circuit as claimed in claim 14, wherein the input line (V_{high}) is permanently high during operation of the circuit.

16. A circuit as claimed in claim 14 or 15, wherein the portion (10) further comprises a reset transistor ($T_{r(n+1)}$) which is connected between the gate of the first input section input transistor and a low power line.

17. A circuit as claimed in any one of claims 5 or 10 to 16, wherein the portion (10) further comprises a feedback reset transistor ($T_{r(n)}$) having its gate connected to the output of the input section stage, for discharging the second input section bootstrap capacitor (C_3).

18. A circuit as claimed in any preceding claim, wherein the input section and the output section of each stage have the same circuit elements, and wherein:

in the input section (60), the input section inputs derived from other input section outputs are provided as feedback paths, and wherein

in the output section (62), the output section inputs derived from other input section outputs are provided as direct paths between the input and output sections.

19. A circuit as claimed in any preceding claim, wherein the input section and the output section share common clock signals (Pn, invPn).

20. A circuit as claimed in any one of claims 1 to 17, wherein the input section and the output section have different clock signals, the clock signals of the output section being used to implement a partial output scheme.

21. A circuit as claimed in any preceding claim, implemented using amorphous silicon technology.

22. An active matrix display device, comprising:

an array (84) of active matrix display pixels;

row driver circuitry (80) comprising a shift register circuit as claimed in any preceding claim.

23. An active matrix display device as claimed in claim 22, comprising an active matrix liquid crystal display device.

24. A method of generating multiple stage shift register circuit outputs for providing a signal to an output load (64), comprising, for each stage of the shift register circuit:

controlling an input section (60) to couple a first clocked power line voltage (Pn) to the output of the input section (60), compensating for the effects of a parasitic capacitance of a drive transistor (T_{drive}) , using the output (R_{n-1}) of the stage one or more stage before the stage to charge the gate of the drive transistor through an input transistor (T_{in1}) and to charge a first bootstrap capacitor (C_2) storing the gate-source voltage of the drive transistor; and

controlling an output section (62) using the outputs of the input sections as timing signals for generating output signals to the output loads.

25. A method as claimed in claim 24, wherein controlling the input section (60) comprises using the output (R_{n-2}) of the stage two ore more stages before the stage to charge the gate of an input transistor (T_{in1}), and storing the gate-source voltage on a second bootstrap capacitor (C_3); and

coupling a first clocked power supply line voltage (Pn) to the output of the stage through the drive transistor.

26. A method as claimed in claim 24 or 25, wherein controlling the output section comprises coupling a second clocked power line voltage to the output of the output section, compensating for the effects of a parasitic capacitance of a drive transistor, using the output of the stage one or more stage before the stage to charge the gate of the drive transistor through an input transistor and to charge a first bootstrap capacitor storing the gate-source voltage of the drive transistor.